Potentialities of Common-used TDC Chips for High-Speed Event Timer Design

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Abstract

Potentialities and drawbacks of the off-the-shelf Time-to-Digital Converter (TDC) chips for building high-speed event timers are considered. To overcome the main shortcoming of TDCs, which is their limited measured interval range, a new technique to obtain the continuous and unlimited time scale is proposed and realized in a pilot version of a TDC-based high-speed event timer. The performance parameters of the pilot device such as RMS resolution vs. aggregate input event rate, non-linearity of time interval measurement between adjacent events, and non-linearity of event instance measurement have been evaluated. It is noted that, although the results show applicability of TDC chips for Laser Ranging related applications, the performance of the TDCs is still not up to the mark and might be improved.

Introduction

During last years the chips called Time-to-Digital Converters (TDC) became available on the market. Such chips provide time interval measurements with high event rate and multiple input channels with independent control. The independent channels allow measuring very short time intervals between Start and Stop events, including small negative time intervals. The chips employ digital interpolation circuitry, which allows achieving a very short dead time for each input channel. As a rule the dead time is limited by maximum write rate of internal buffer memory. Some TDC chips have arithmetic logic unit that are used for interpolation data preprocessing, including the averaging of results to increase the precision.

One of the best TDC products is the chip TDC-GPX from ACAM Mess-electronic Gmbh. It offers several modes with different resolution and available number of channels. The mode with 8 LVTTL channels for Stop events offers typical RMS resolution of 81 ps and up to 182 MHz burst event rate for each channel (up to 32 events in one burst). Continuous average aggregate (for all channels) event rate in this mode is up to 40 MHz. Such rate can be supported by employing fast PC buses or new generation interfaces, for example USB 3.0. For lower average aggregate rates up to 15 MHz could be used existing interfaces: USB 2.0, FireWire. In the most accurate measurement mode only two LVPECL differential inputs for Stop events are available. In this mode 10 ps RMS resolution can be obtained - although, at relatively low event rate (up to 500 KHz).

The main drawback of TDC chips is that they are implemented according to the traditional time interval measurement technique and have a limited time interval measurement range. It means that they cannot be used directly to build true Event Timers. The goal of this work was to solve that problem and develop a high-speed TDC-GPX-based Event Timer with unlimited time range. The other goal was to evaluate potentialities and actual performance of such Event Timers.

Constructing of Unlimited Single-valued Time Scale

To solve the problem of the limited measurement range the manufacturer of TDC-GPX offered the possibility of an internal Start generation with controlled periodicity for a time counter re-triggering. Additional Restart counter allows to extend the measurement range up to 1.28 ms. The simplified block diagram of this mechanism is shown in Fig. 1.

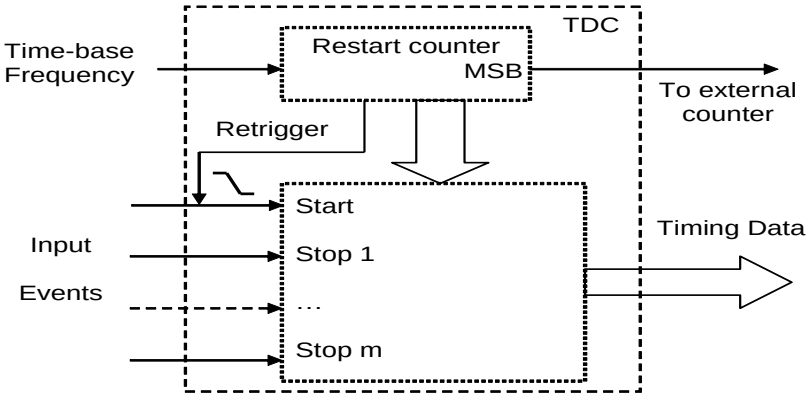

Figure 1. A TDC with Additional Restarting Circuitry

The manufacturer suggested to count the most significal bit (MSB, Fig.1) changes in the external counter to get the unlimitted measurement range. Such simple way to extend the range can not be easily realized due to the problems with correct data reading, especially at high event rates. Indeed, if the user just directly employs an external counter, the state of the counter should be read at the moments when the input events arrive. It may lead to errors of association between codes that are written into the internal FIFO and those read from the external counter (so-called timing uncertainty) into some external FIFO. Even if such design is done correctly, with the use of a proper circuitry of timing uncertainty ellimination, it nevertheless is bulky and may degrade the accuracy performance of a timer. Besides, the amount of data to be transferred increases according to the required time scale extension length. And finally, the timeless measurement range cannot be obtained at all.

To solve this problem we have come to a different solution (Artyukh[1], 2008). One measurement input of the TDC was assigned as a specific marker input (see Fig. 2). The MSB signal of the restart counter is delayed (to avoid any timing uncertainty (Беспалько, 1985)) and then is fed into this input. The marker input is configured for accepting both positive and negative edges. In this way we insert specific marker events, corresponding to transitions of the MSB of the restart counter, into the output digital data stream that is transmitted further (into some controller block based on μC, CPLD or FPGA).

The constructing of single-valued time scale could be done either by the controller block firmware or by PC software where the data finally come in most of applications. The firmware or software detects the marker measurement data blocks and constructs the extension time scale simply as a variable to use for composing resultant time stamps. When it is done on a PC, this solution not only allows constructing practically limitless single-valued time scale by means of software but also substantially reduces the amount of transferred data for high rate event streams.

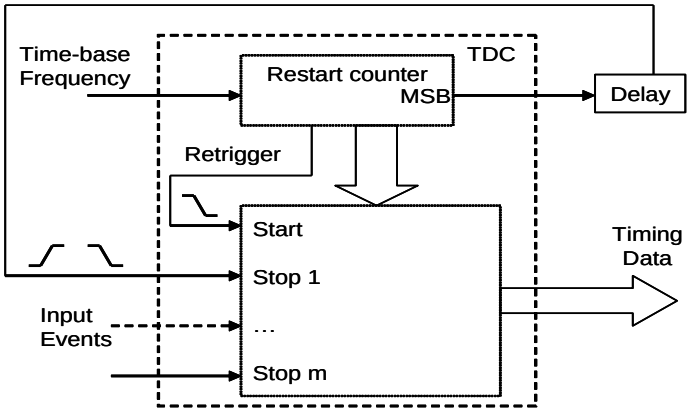

Figure 2. A TDC with Restarting and Marker Event Insertion Circuitry

Event Timer Implementation

The described method was realized in a pilot model of 6-channel High Speed Event Timer (HSET) with unlimited range of time measurements. The HSET Block diagram is shown in the Fig.3. HSET employs the TDC-GPX as its main measurement core. All settings and data exchange in accordance with the TDC-GPX functionality and controls functions, issued from the PC, are implemented by a control block, which is written in VHDL and realized on a Cyclone II FPGA from Altera Corp. USB chip (CY7C68013A from Cypress Semiconductor Corp.) memory is used as a buffer memory for control data transfer into TDC-GPX and for measurement data accumulation. The HSET is a PC based instrument and communicating with the PC is done via USB port (USB 2.0 High Speed).

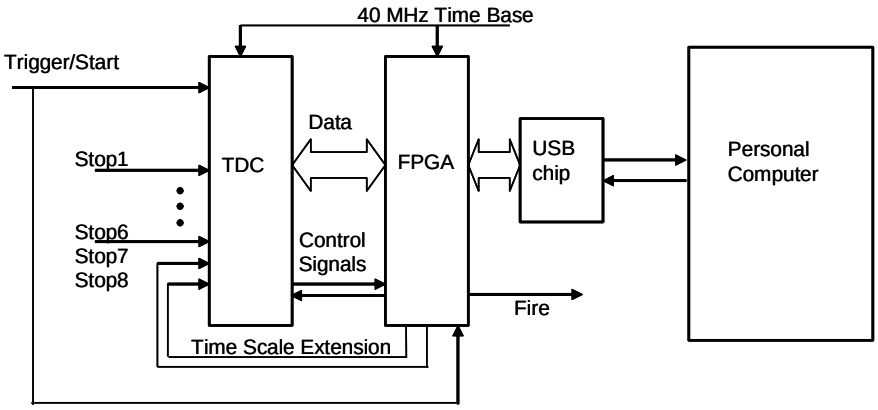

Figure 3. HSET Block Diagram

PC software for interacting with the HSET is written in C under National Instruments LabWindows/CVI. The latter includes means for USB interface configuring, programming, and interacting according to the Virtual Instrument Software Architecture. Specialized HSET software comprises program functions that support control and data read operations for HSET. These functions can be incorporated into application-specific timing system. They were included into the programs for evaluating the HSET performance characteristics. The methods and techniques for performance evaluation were presented in (Artyukh[2], 2008; Boole, 2007).

Photography of the HSET front view is shown in Fig. 4. There are 4 input channels and Trigger/Start input on the front panel. Two more channels, time-base input and some additional connectors are placed on the rear panel.

Figure 4. A Photo of HSET

Evaluation of HSET Characteristics

To evaluate the RMS resolution of HSET a direct repetitive measurement of test signal with low jitter was performed. The generator (ROHDE&SCHWARZ SML 02) was used to generate a stable signal with RMS jitter less than 10 ps. This signal was connected to one channel, then it was split into two and four channels for increasing the burts aggregate event rate up to 600 millions events per second.

In the process of HSET evaluation it was noticed that its RMS resolution considerably varies from 60 ps to 310 ps depending on the amount of employed channels and the aggregate event rate (see Fig. 5). The main reason of the resolution degradation is the on-chip PLL performance degradation caused by internally induced noises, especially at high-intensity bursts.

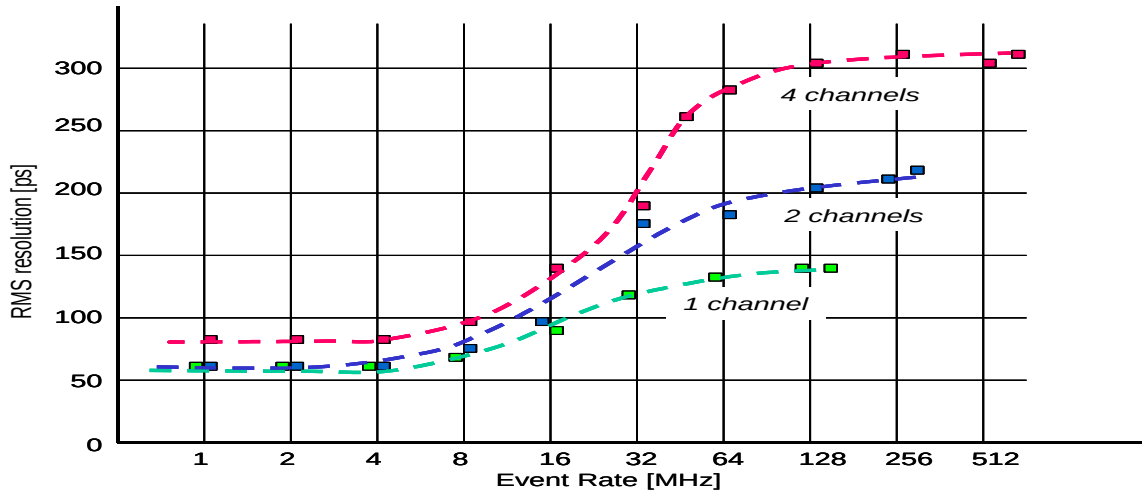

Figure 5. RMS Resolution vs. Aggregate Input Event Rate

It was anticipated that there should be cross correlation between events coming in different channels in the case of short time intervals between them. The statistical testing approach [3] shows that such correlation exists and causes noticeable non-linearity of time interval measurement between adjacent events (see Fig. 6).

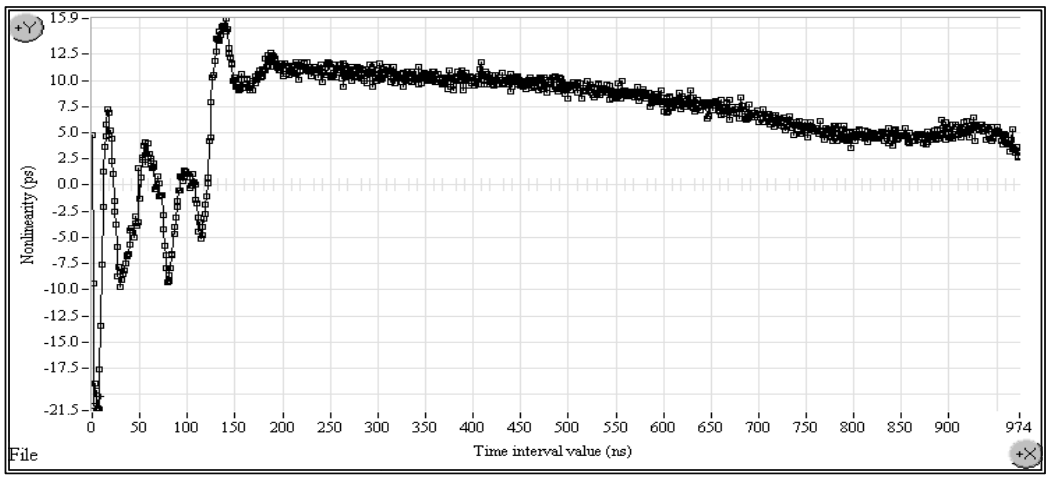

Figure 6. Non-linearity of Time Interval Measurement

Taking into account, that the RMS resolution of the timer is about 60-90 ps at low and medium aggregate input event rate (up to 6…8 MHz), the non-linearity error is regarded as settled and non-essential for intervals more than 150-200 ns.

One of the components of RMS resolution is the integral nonlinearity of the timer [4]. Noticable dependence of the event instant measurement error on the instant relative position within the interpolation interval was detected in the process of integral nonlinerity evaluation of HSET.

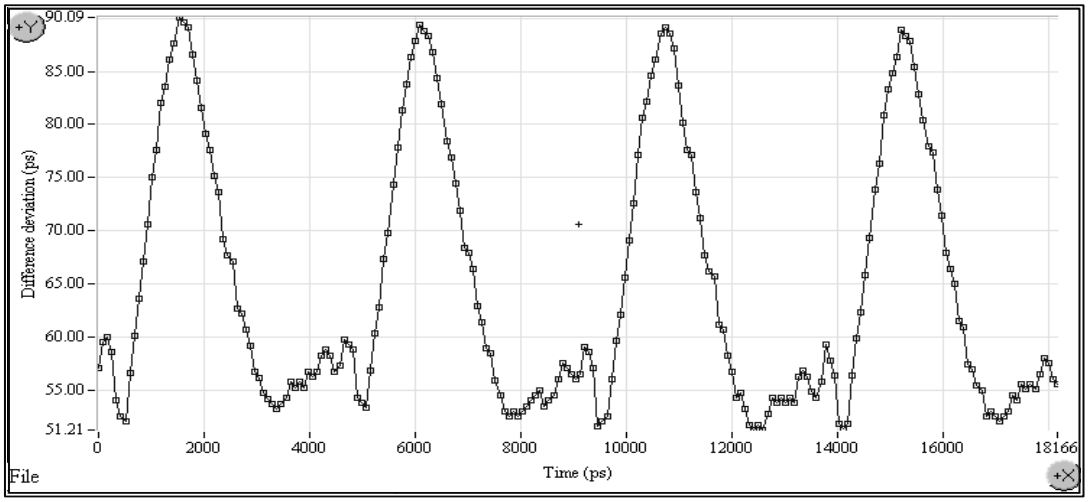

Figure 7. Non-linearity of Time Measurement

The graph in Fig.7 reflects the non-linearity of the TDC-GPX discrete interpolator over 4 periods of its operation. The peak-to-peak non-linearity error is about 40 ps and it is one of the error components of the evaluated RMS resolution.

Conclusions

Generally it can be concluded that some of currently available commercial TDC chips (such as TDC-GPX) are applicable for event timer designs that target the applications where compact implementation and high rate of multi-channel event timing are mostly needed.

As for the achievable resolution, it is not up to the mark (especially at very high event rates); the existing limitations are caused by imperfectness of TDC-chip realization. It seems that a custom design of a TDC chip, specificlly tailored for building the true event timers (in cooperation with a manufacturer), may lead to much better results.

The High-Speed Event Timer designed in the framework of the presented research offers a good price/performance ratio as compared to the commercially available devices of such kind. We hope that this can make it (or its options) attractive for the applications related to Laser Ranging.

References

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